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FEE TRANSMITTAL

Patent fees are subject to annual revision.

Complete If Known	
Application Number	09/832,200
Filing Date	11 April 2001
First Named Inventor	CHUL-MIN KIM
Examiner Name	SHIBRU, HELEN
Group/Art Unit	2621
Attorney Docket No.	P56349

TOTAL AMOUNT OF PAYMENT ($) 500.00

METHOD OF PAYMENT (check one)

1. ■ **Payment Enclosed: (CHECK #51302)**
   ■ Check ❑ Credit Card ❑ Money Order
   ❑ Other

❑ Charge Any Additional Fee Required Under 37 C.F.R. §1.16 and 1.17.

❑ Applicant claims small entity status. See 37 CFR 1.27

2. ■ The Commissioner is hereby authorized to charge any deficiency and credit any over payments to:

Deposit Account Number: 02-4943

FEE CALCULATION

Fee Code	Fee ($)	Fee Code	Fee ($)	Fee Description	Fee Paid
EXTENSION OF TIME FEES					
1251	120	2251	60	Extension for reply within first month	$
1252	450	2252	225	Extension for reply within second month	$
1253	1020	2253	510	Extension for reply within third month	$
1254	1590	2254	795	Extension for reply within fourth month	$
1255	2160	2255	1080	Extension for reply within fifth month	$
APPEAL					
1401	500	2401	250	Notice of Appeal	$
1402	500	2402	250	Filing a brief in support of an appeal	$ 500.00
1403	1000	2403	500	Request for oral hearing	$
CLAIMS					
1201	200	2201	100	Independent claims in excess of 3	$
1202	50	2202	25	claims in excess of 20	$
Other Fee (specify) _____					$
Other Fee (specify) _____					$
Other Fee (specify) _____					$

FEE CALCULATION

Fee Code	Fee ($)	Fee Code	Fee ($)	Fee Description	Fee Paid
MISCELLANEOUS					
1801	$790	2801	$395	Request for continued examination (RCE)	$
1806	$180			Submission of an IDS	$
1814	$130	2814	$65	Statutory disclaimer	$
8021	$40			Recordation of assignment per property	$
TRADEMARK					
6001/7001			$335	Application for registration, per class	$
6002/7002			$100	Amendment to Allege Use, per class	$
6003/7003			$100	Statement of Use, per class	$
6004/7004			$150	Request for six-month extension of time, per class	$
6205/7205			$100	§8 affidavit, per class	$
6208/7208			$200	§15 affidavit, per class	$
6201/7201			$400	Application for renewal, per class	$
6403/7403			$100	Ex parte appeal, per class	$
PETITION					
1462			$400	Petitions to Director (Group I)	$
1463			$200	Petitions to Director (Group I)	$
1464			$130	Petitions to Director (Group II)	$
1452	$500	2452	$250	Petitions to revive unavoidably abandoned application	$
1453	$1500	2453	$750	Petitions to revive unintentionally abandoned application	$
PATENT MAINTENANCE					
1551	$900	2551	$450	Due at 3.5 years	$
1552	$2300	2552	$1150	Due at 7.5 years	$
1553	$3800	2553	$1900	Due at 11.5 years	$
Other Fee (specify) _____					$
Other Fee (specify) _____					$
Other Fee (specify) _____					$

SUBTOTAL: LEFT COLUMN	$ 500.00	SUBTOTAL: RIGHT COLUMN	$ 0.00

SUBMITTED BY

Typed or Printed Name	Robert E. Bushnell, Esq.	Reg. Number	27,774
Signature		Date	24 August 2006
Deposit Account User ID			

REB/ks

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCES

In re Application of:

Appeal No. _____

CHUL-MIN KIM

Serial No.:	09/832,200	Examiner:	SHIBRU, HELEN
Filed:	11 April 2001	Art Unit:	2621

For: METHOD FOR DESIGNING ENVELOPE DETECTING CIRCUIT FOR VIDEO SIGNAL PROCESSING INTEGRATED CIRCUIT AND INTEGRATED CIRCUIT USING THE SAME

Attn: Board of Patent Appeals & Interferences

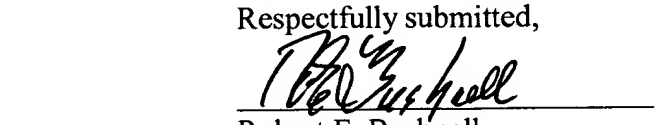
TRANSMITTAL OF APPELLANT'S BRIEF FEE

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Sir:

Accompanying this transmittal is a check drawn to the Commissioner of Patents & Trademarks in the amount of $500.00 (Check #51302) for the filing an **Appeal Brief** in support of a Notice of Appeal filed on 26 June 2006. Should the check become lost, be deficient in payment, or should other fees be incurred, the Commissioner is authorized to charge Deposit Account No. 02-4943 of Applicant's undersigned attorney in the amount of such fees.

Respectfully submitted,



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Washington, D.C. 20005
Area Code: 202-408-9040

Folio: P56349
Date: 8/24/06
I.D.: REB/ks

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCES

In re Application of:

Appeal No. _____

CHUL-MIN KIM

Serial No.: 09/832,200 Examiner: SHIBRU, HELEN

Filed: 11 April 2001 Art Unit: 2621

For: METHOD FOR DESIGNING ENVELOPE DETECTING CIRCUIT FOR VIDEO SIGNAL PROCESSING INTEGRATED CIRCUIT AND INTEGRATED CIRCUIT USING THE SAME

APPEAL BRIEF

Paper No. 10

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to Appellant's Notice of Appeal filed on 26 June 2006, Appellant hereby appeals to the Board of Patent Appeals and Interferences from the final rejection of claims 1 thru 7, 10 thru 17 and 20 as set forth in the final Office action mailed on 25 January 2006 (Paper No. 20060120).

Claims 8, 9, 18 and 19 have been allowed as set forth in Paper No. 20060120.

Folio: P56349
Date: 8/24/06
I.D.: REB/JGS/kf

08/25/2006 JADD01 00000016 09832200
01 FC:1402 500.00 OP

I. REAL PARTY IN INTEREST

Pursuant to 37 CFR §41.37 (as amended), the real party in interest is:

SamSung Electronics Co., Ltd.
#416, Maetan-dong, Yeongtong-gu,
Suwon-si, Gyeonggi-do, 442-742, Republic of KOREA

as evidenced by the Assignment executed by the inventor on 9 April 2001 and recorded in the U.S. Patent & Trademark Office on 11 April 2001 at Reel 011716, frame 0618.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals and no interferences known to Appellant, Appellant's legal representatives or the assignee which will directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1 thru 7, 10 thru 17 and 20 stand finally rejected. Of the latter claims, claims 1, 5, 11 and 15 are independent, whereas the remaining claims are dependent. Claims 8, 9, 18 and 19 are allowed as stated in the final Office action (Paper No. 20060120).

IV. STATUS OF AMENDMENTS

There is no Amendment filed subsequent to the final rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to a video signal processing integrated circuit (IC) and an IC designing method and, more particularly, to a method for designing an envelope detecting circuit for a video signal processing IC in order to reduce operating steps and material costs by minimizing the number of components of external application circuits of the video signal processing IC, and to an IC using the method.

In the method of the present invention, the number of peripheral components of the video signal processing IC is minimized by incorporating, into the video signal processing IC, a circuit device for detecting the envelope of an FM video signal and for controlling the envelope level. According to the IC designing method, the number of components can be reduced by designing all circuit elements constituting a circuit which detects the envelope of the FM video signal and which controls envelope level so that they are incorporated into the video signal processing IC at the time of designing the video signal processing IC. As a result, cost is reduced and, since mode control signal lines are reduced, the corresponding terminals of the microprocessor can be used for another purpose, thereby increasing the operating efficiency of the microprocessor.

As recited in independent claim 1, with reference to Figure 2, the invention relates to a method of designing a video signal processing integrated circuit (IC), comprising the steps of: providing the video signal processing IC 240 with an envelope detector 241 for detecting and outputting an envelope of a frequency modulated (FM) video signal; providing the video signal processing IC 240 with a level variation switching circuit 241c for changing an envelope level of the

FM video signal; and connecting an input of the level variation switching circuit 241c to a control output of a microprocessor 242 so that ON/OFF switching control of the level variation switching circuit 241c is executed in response to a control data input from the microprocessor 242.

As recited in independent claim 5, with reference to Figure 2, the invention relates to a video signal processing integrated circuit (IC) 240 incorporating an envelope detecting circuit 241 for detecting an envelope level of an FM video signal, wherein the envelope detecting circuit 241 comprises: a peak detector 241b for receiving the FM video signal and for detecting a peak value of the FM video signal; and a level switch 241c having a first input connected to an output of the peak detector 241b and having a second input connected to a control output of a microprocessor 242 for controlling the envelope level of the FM video signal according to mode information applied from the microprocessor 242 so as to reduce a variation in the envelope level in accordance with a type of mode of operation of a video cassette recorder (VCR).

As recited in independent claim 8, with reference to Figures 2 and 3, the invention relates to a video signal processing integrated circuit (IC) 240 incorporating an envelope detecting circuit 241 for detecting an envelope level of an FM video signal, wherein the envelope detecting circuit 241 comprises: a peak detector 241b for receiving the FM video signal and for detecting a peak value of the FM video signal; and a level switch 241c connected to an output of the peak detector 241b for controlling the envelope level of the FM video signal according to mode information applied from a microprocessor 242 so as to reduce a variation in the envelope level in accordance with a type of

mode of operation of a video cassette recorder (VCR); wherein the level switch 241c includes a resistance element R37 having a first terminal connected to the output of the peak detector 241b and having a second terminal, and a switching control element Q32 connected to the second terminal of the resistance element R37, the switching control element Q32 being controlled by the mode information SP'H' from the microprocessor 242.

As recited in independent claim 11, with reference to Figure 2, the invention relates to a method of designing a video signal processing integrated circuit (IC) 240 having an envelope detector 241 for detecting an envelope of a frequency modulated (FM) video signal, the method comprising the steps of: providing a level variation switching circuit 241c in the video signal processing IC 240 for changing an envelope level of the FM video signal according to an execution mode; connecting an input of the level variation switching circuit 241 to a control output of a microprocessor 242; and providing an ON/OFF switching control of the level variation switching circuit 241 in response to a control data input from the microprocessor 242, said control data input containing playback mode information relative to the FM video signal.

As recited in independent claim 15, with reference to Figure 2, the invention relates to a video signal processing circuit 240 for detecting an envelope level of an FM video signal input thereto, the circuit 240 comprising: peak detector means 241b for receiving the FM video signal and for detecting a peak value of the FM video signal; and level switch means 241c connected to said peak detector means 241b for controlling the envelope level of the FM video signal according to

playback mode information relating to a mode of operation of a video cassette recorder (VCR), said playback mode information being applied to said level switch means 241c so as to reduce a variation in the envelope level in accordance with the mode of operation of the video cassette recorder (VCR).

Finally, as recited in independent claim 18, with reference to Figures 2 and 3, the invention relates to a video signal processing circuit 240 for detecting an envelope level of an FM video signal input thereto, the circuit 240 comprising:

peak detector means 241b for receiving the FM video signal and for detecting a peak value of the FM video signal; and

level switch means 241c connected to said peak detector means 241b for controlling the envelope level of the FM video signal according to mode information applied thereto so as to reduce a variation in the envelope level in accordance with a mode of operation of a video cassette recorder (VCR);

wherein said level switch means 241c includes a resistance element R37 having a first terminal connected to said peak detector means 241b and having a second terminal, said level switch means 241c further including a switching control element Q32 connected to the second terminal of the resistance element R37, the switching control element Q32 being controlled by the mode information applied to said level switch means 241c.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1 thru 7, 10 thru 17 and 20 are improperly rejected under 35 U.S.C. §103 for alleged unpatentability over Jeong *et al.*, U.S. Patent No. 5,218,489 in view of Kubota, U.S. Patent No. 5,359,428.

VII. ARGUMENT

Grouping of claims

Claim 1;

Claim 2;

Claim 3;

Claim 4;

Claim 5;

Claim 6;

Claim 7;

Claim 10;

Claim 11;

Claim 12;

Claim 13;

Claim 14;

Claim 15;

Claim 16;

Claim 17; and

Claim 20.

Justification of Grouping of claims

Independent claim 1 is separately grouped by virtue of its recitation of a method of designing a video signal processing integrated circuit comprising the combination of the three steps recited in claim 1.

Dependent claim 2 is separately grouped from independent claim 1 by virtue of its recitation of a method wherein the level variation switching circuit reduces variation in the envelope level of the FM video signal according to standard playback (SP) mode information and super long playback (SLP) mode information, respectively, contained in the control data input from the microprocessor.

Dependent claim 3 is separately grouped from independent claim 1 by virtue of its recitation of a method wherein the level variation switching circuit operates in dependence on a playback mode of a video cassette recorder.

Dependent claim 4 is separately grouped from independent claim 1 by virtue of its recitation of a method wherein the level variation switching circuit has a resistor at an output terminal of the envelope detector.

Independent claim 5 is separately grouped by virtue of its recitation of a video signal processing integrated circuit incorporating an envelope detecting circuit, the envelope detecting circuit comprising a peak detector and a level switch having the respective functions recited in claim 5.

Dependent claim 6 is separately grouped from independent claim 5 by virtue of its recitation of a video signal processing integrated circuit which further comprises an amplifier connected to an input terminal of the peak detector for performing the function recited in claim 6.

Dependent claim 7 is separately grouped from independent claim 5 by virtue of its recitation of a video signal processing integrated circuit which further comprises an amplifier connected to an output terminal of the peak detector for performing the function recited in claim 7.

Dependent claim 10 is separately grouped from independent claim 5 by virtue of its recitation of mode information comprising SP/SLP mode information relating to operation of the VCR.

Independent claim 11 is separately grouped by virtue of its recitation of a method of designing a video signal processing integrated circuit having an envelope detector for detecting an envelope of a frequency modulated video signal, the method comprising the combination of the three step recited in claim 11.

Dependent claim 12 is separately grouped from independent claim 11 by virtue of its recitation of the further step of providing the level variation switching circuit with a capability of reducing variation in the envelope level of the FM video signal according to standard playback (SP) mode information and super long playback (SLP) mode information, respectively, contained in the control data input from the microprocessor.

Dependent claim 13 is separately grouped from independent claim 11 by virtue of its recitation of the level variation switching circuit operating in dependence on a playback mode of a video cassette recorder.

Dependent claim 14 is separately grouped from independent claim 11 by virtue of its recitation of the level variation switching circuit having a resistor at an output terminal of the envelope detector.

Independent claim 15 is separately grouped by virtue of its recitation of a video signal processing circuit for detecting an envelope level of an FM video signal input thereto, the circuit comprising the combination of peak detector means and level switch means having the respective functions recited in claim 15.

Dependent claim 16 is separately grouped from independent claim 15 by virtue of its recitation of the video signal processing circuit as further comprising an amplifier connected to an

input terminal of the peak detector means for amplifying the FM video signal with a predetermined gain prior to provision to the peak detector means.

Dependent claim 17 is separately grouped from independent claim 15 by virtue of its recitation of a video signal processing circuit further comprising an amplifier connected to an output terminal of the peak detector means for amplifying the FM video signal with a predetermined gain after processing in the peak detector means.

Dependent claim 20 is separately grouped from independent claim 15 by virtue of its recitation of the mode information as comprising SP/SLP mode information relating to the operation of a VCR.

Patentability Over the Prior Art

In rejecting independent 1, the Examiner cites Jeong *et al.* '489 as disclosing a video signal processing circuit having an envelope detector, the Examiner citing the envelope detector 200 of Figures 2 and 3 of Jeong *et al.* '489. The Examiner then cites the comparator 300 and second amplifier 450 of Figures 2 and 3 of Jeong *et al.* '489 as corresponding to the claimed level variation switching circuit "for changing an envelope level of the FM video signal (the video signal detected by the reproducing head HD and that supplies to the comparator (300)" (quoting from the last two lines on page 2 of the final Office action). However, the comparator 300 and second amplifier 450 do not perform the function of the level variation switching circuit, as that function is recited in

independent claim 1.

In the latter regard, Jeong *et al.* '489 discloses that the comparator 300 compares a signal from the second amplifier 450 with the signal from a waveform shaper 230, and supplies the compared data D to the microcomputer 400 (*see* column 2, lines 54-57 of Jeong *et al.* '489). Therefore, the comparator 300 and the second amplifier 450 cited by the Examiner do not perform the function of "changing an envelope level of the FM video signal" as recited in independent claim 1 (line 6 thereof); rather, they merely generate a comparison signal or "compared data" D.

Jeong *et al.* '489 then discloses that, in the microcomputer 400, the output signal D of the comparator 300 is "stepped up or down based on the duty ratio difference supplied by one step, and the resulting tracking control data is supplied to the servo stage 500, so that the tracking is automatically controlled" (quoting from column 3, lines 56-60 of Jeong *et al.* '489). Thus, if the Examiner is contending that the function of stepping up or stepping down the output signal D of the comparator 300 corresponds to the recited function of "changing an envelope level of the FM video signal" (as recited in independent claim 1, line 6), then the microcomputer 400 must necessarily be a part of the combination of elements corresponding to the recited level variation switching circuit. That is to say, the element of Jeong *et al.* '489 corresponding to the recited level variation switching circuit must include not only the comparator 300 and the second amplifier 450, but also the microcomputer 400.

Referring to the last step of the method recited in independent claim 1, that step consists of "connecting an input of the level variation switching circuit to a control output of a microprocessor so that ON/OFF switching control of the level variation switching circuit is executed in response to a control data input from the microprocessor" (quoting from the last three lines of independent claim 1). Therefore, since the microcomputer 400 of Jeong *et al.* '489 must necessarily be a part of the combination cited by the Examiner as corresponding to the recited level variation switching circuit, the microcomputer 400 cannot correspond to the microprocessor recited in the last step of independent method claim 1. Moreover, it is clear, in any event, that the microcomputer 400 does not perform ON/OFF switching control of the level variation switching circuit, as admitted by the Examiner in the second paragraph on page 3 of the final Office action.

In that regard, the Examiner cites Kubota *et al.* '428 as allegedly disclosing a tape speed selector to record a signal at an appropriate speed, the Examiner further asserting that Kubota *et al.* '428 "discloses connecting an input of the level variation switching circuit (see fig. 8 SP/LP select (55)) to a control output of a microprocessor so that ON/OFF switching control of the level variation switching circuit is executed in response to a control data input from ((a)) the microprocessor (see input terminal (56)in fig. 8 and col. 11 lines 54-64 and col. 12 lines 17-54)" (quoting from the third paragraph on page 3 of the final Office action). Applicant respectfully disagrees with this analysis and the alleged disclosure of a level variation switching circuit in Kubota *et al.* '428 for the following reasons.

First, the element 55 of Figure 8 of Kubota *et al.* '428, cited by the Examiner, is merely an SP/LP select switch, that is, a mode selector switch by means of which a user may manually or a processor may automatically designate the speed at which a video tape is played or recorded, "SP" designating "short play" and "LP" designating "long play" (*see* column 11, lines 54-57 of Kubota '428).

Second, it should be noted that the mode selector 55 does not produce an output which will perform ON/OFF switching control of a level variation switching circuit since the output of the mode selector 55 (in Figure 8 of Kubota *et al.* '428) is merely connected to a summing circuit 54. Thus, the arrangement of Figure 8 of Kubota *et al.* '428 is an entirely different arrangement relative to the arrangement disclosed in Jeong *et al.* '489.

Since the arrangement of Kubota *et al.* '428 is an entirely different arrangement relative to the arrangement disclosed in Jeong *et al.* '489, it is highly doubtful that one of ordinary skill in the art, upon reviewing the disclosure of Jeong *et al.* '489, would be led to the disclosure of Kubota *et al.* '428 for the purpose of modifying the disclosure of Jeong *et al.* '489. It is respectfully submitted that the only reason that the Examiner has been led to the disclosure of Kubota *et al.* '428 is that the Examiner has had the benefit of reviewing the disclosure of the present application which, of course, would not be available to a person of ordinary skill in the art as of the date of the invention.

Furthermore, even if the combination of Jeong *et al.* '489 and Kubota *et al.* '428 would be

obvious or available to a person of ordinary skill in the art as of the date of the invention, the combination of those two references, or the modification of Jeong *et al.* '489 in accordance with the disclosure of Kubota *et al.* '428, would not result in the present invention, as claimed. Specifically, if one were to take the mode selector 55 of Figure 8 of Kubota *et al.* '428, and substitute it for the combination of the comparator 300, microcomputer 400 and amplifier 450 of Figure 2 of Jeong *et al.* '489, one would still not obtain an arrangement comprising a level variation switching circuit for changing an envelope level of an FM video signal, as recited in claim 1, and one would also not obtain an arrangement wherein an input of a level variation switching circuit is connected to a control output of a microprocessor so that ON/OFF switching control of a level variation switching circuit is executed in response to a control data input from the microprocessor, as recited in the last two paragraphs of independent claim 1.

For the latter reasons, the invention recited in independent claim 1 is distinguishable from the prior art cited by the Examiner so as to preclude rejection under 35 U.S.C.§103.

With respect to dependent claims 2 and 3, the Examiner's rejection is based primarily on the statement contained in the last paragraph on page 4 of the final Office action, in which the Examiner alleges that "Kubota discloses the level variation switching circuit reduces variation in the envelope level of the FM video signal", the Examiner referring to the mode selector 55 of Figure 8 of Kubota *et al.* '428. However, as pointed out above, the element 55 of Figure 8 of Kubota *et al.* '428 is clearly a mode selector switch which merely sends a signal to the summer circuit 54 designating

whether a "short play" or a "long play" speed for operation of a video tape recorder has been selected by a user or by a microprocessor.

With respect to dependent claim 4, the Examiner alleges that Jeong *et al.* '489 discloses a level variation switching circuit having a resistor at an output terminal of the envelope detector, the Examiner referring to the resistor VR in Figure 2 of Jeong *et al.* '489, as well as column 2, line 66 - column 3, line 6 of the patent. However, given the fact that the Examiner alleges that the comparator 300 and amplifier 450 of Figure 2 of Jeong *et al.* '489 correspond to the recited level variation switching circuit (note that, as stated above, microcomputer 400 should also be a part of that combination), the resistor VR connected between the power source Vcc and the switch SW1 is not connected to an **output** terminal of the combination which the Examiner alleges to correspond to the level variation switching circuit. Rather, the variable resistor VR is connected to an input terminal of the microcomputer 400. Moreover, the resistor VR is connected to the input terminal only when the switch SW1 is moved to the "manual" position. Thus, the variable resistor VR of Figure 2 of Jeong *et al.* '489 does not correspond to the resistor recited in dependent claim 4.

Turning to consideration of independent claim 5, that claim recites a video signal processing integrated circuit (IC) corresponding to the circuit recited as a part of independent method claim 1 discussed above. Thus, the Examiner rejects independent claim 5 on the same basis as independent 1 is rejected. For that reason, the arguments set forth above relative to the patentability of independent claim 1 are applicable to the question of patentability of independent claim 5.

Therefore, the invention recited in independent claim 5 is distinguishable from the prior art cited by the Examiner on the same basis, as set forth above, that the invention of independent claim 1 is distinguishable over the prior art cited by the Examiner.

On page 6 of the final Office action, the Examiner states that dependent claim 10 is rejected for the same reason as discussed with respect to dependent claims 2 and 3. Therefore, the arguments set forth above relative to dependent claims 2 and 3 are applicable to the question of patentability of dependent claim 10.

At the bottom of page 6 of the final Office action, the Examiner states that the limitations of independent 11 can be found in independent claim 1 and associated dependent claims 2 and 3. Therefore, the Examiner states that independent claim 11 is rejected for the same reasons as discussed with respect to claims 1 thru 3. Accordingly, the arguments set forth above relative to independent claim 1 and associated dependent claims 2 and 3 apply equally to the question of the patentability of the invention recited in independent claim 11. Therefore, the invention recited in independent claim 11 is distinguishable from the prior art cited by the Examiner for the same reasons as set forth above relative to claims 1 thru 3.

At the top of page 7 of the final Office action, the Examiner states that the limitations of dependent claims 12 and 13 can be found in dependent claims 2 and 3, and therefore the Examiner rejects dependent claims 12 and 13 for the same reasons as discussed with respect to claims 2 and

3. Accordingly, the arguments set forth above relative to dependent claims 2 and 3 apply equally to the question of the patentability of the invention recited in dependent claims 12 and 13, and thus, dependent claims 12 and 13 are patentable for the same reasons as set forth above relative to claims 2 and 3.

Similarly, on page 7 of the final Office action, the Examiner states that dependent claim 14 is rejected for the same reasons as set forth relative to dependent claim 4. Therefore, the invention of dependent claim 14 is patentable for the same reasons as set forth above relative to dependent claim 4.

Finally, on page 7 of the final Office action, the Examiner states that independent claim 15 is rejected for the same reasons as set forth relative to independent claim 5, and the Examiner also states that dependent claims 16, 17 and 20 are rejected for the same reasons as set forth relative to dependent claims 6, 7, and 2 and 3, respectively. Therefore, for the same reasons set forth above relative to dependent claims 6 and 7, as well as dependent claims 2 and 3, the invention of dependent claims 16, 17 and 20 is distinguishable from the prior art cited by the Examiner so as to preclude rejection under 35 U.S.C.§103.

In view of the law and facts stated herein, as well as all of the foregoing reasons, Appellant believes that the rejection is improper, and respectfully requests that the Board refuse to sustain the outstanding rejection of claims 1 thru 7, 10 thru 17 and 20 under 35 U.S.C. §103.

Respectfully submitted,

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Folio: P56349
Date: 8/24/6
I.D.: REB/JGS

VIII. APPENDIX

CLAIMS UNDER APPEAL (1-7, 10-17 and 20)

1. (Previously Presented) A method of designing a video signal processing integrated circuit (IC), comprising the steps of:

providing the video signal processing IC with an envelope detector for detecting and outputting an envelope of a frequency modulated (FM) video signal;

providing the video signal processing IC with a level variation switching circuit for changing an envelope level of the FM video signal; and

connecting an input of the level variation switching circuit to a control output of a microprocessor so that ON/OFF switching control of the level variation switching circuit is executed in response to a control data input from the microprocessor.

2. (Original) The method according to claim 1, wherein the level variation switching circuit reduces variation in the envelope level of the FM video signal according to standard playback (SP) mode information and super long playback (SLP) mode information, respectively, contained in the control data input from the microprocessor.

3. (Original) The method according to claim 1, wherein the level variation switching circuit operates in dependence on a playback mode of a video cassette recorder.

4. (Original) The method according to claim 1, wherein the level variation switching circuit has a resistor at an output terminal of the envelope detector.

5. (Previously Presented) A video signal processing integrated circuit (IC) incorporating an envelope detecting circuit for detecting an envelope level of an FM video signal, wherein the envelope detecting circuit comprises:

a peak detector for receiving the FM video signal and for detecting a peak value of the FM video signal; and

a level switch having a first input connected to an output of the peak detector and having a second input connected to a control output of a microprocessor for controlling the envelope level of the FM video signal according to mode information applied from the microprocessor so as to reduce a variation in the envelope level in accordance with a type of mode of operation of a video cassette recorder (VCR).

6. (Original) The video signal processing IC according to claim 5, further comprising an amplifier connected to an input terminal of the peak detector for amplifying the FM video signal with a predetermined gain prior to provision to the peak detector.

7. (Original) The video signal processing IC according to claim 5, further comprising an amplifier connected to an output terminal of the peak detector for amplifying the FM video signal with a predetermined gain after processing in the peak detector.

10. (Original) The video signal processing IC according to claim 5, wherein the mode information comprises SP/SLP mode information relating to operation of the VCR.

11. (Previously Presented) A method of designing a video signal processing integrated circuit (IC) having an envelope detector for detecting an envelope of a frequency modulated (FM) video signal, said method comprising the steps of:

providing a level variation switching circuit in the video signal processing IC for changing an envelope level of the FM video signal according to an execution mode;

connecting an input of the level variation switching circuit to a control output of a microprocessor; and

providing an ON/OFF switching control of the level variation switching circuit in response to a control data input from the microprocessor, said control data input containing playback mode information relative to the FM video signal.

12. (Original) The method according to claim 11, further comprising the step of providing the level variation switching circuit with a capability of reducing variation in the envelope level of the FM video signal according to standard playback (SP) mode information and super long playback (SLP) mode information, respectively, contained in the control data input from the microprocessor.

13. (Original) The method according to claim 11, wherein the level variation switching

circuit operates in dependence on a playback mode of a video cassette recorder.

14. (Original) The method according to claim 11, wherein the level variation switching circuit has a resistor at an output terminal of the envelope detector.

15. (Previously Presented) A video signal processing circuit for detecting an envelope level of an FM video signal input thereto, said circuit comprising:

peak detector means for receiving the FM video signal and for detecting a peak value of the FM video signal; and

level switch means connected to said peak detector means for controlling the envelope level of the FM video signal according to playback mode information relating to a mode of operation of a video cassette recorder (VCR), said playback mode information being applied to said level switch means so as to reduce a variation in the envelope level in accordance with the mode of operation of the video cassette recorder (VCR).

16. (Original) The video signal processing circuit according to claim 15, further comprising an amplifier connected to an input terminal of said peak detector means for amplifying the FM video signal with a predetermined gain prior to provision to said peak detector means.

17. (Original) The video signal processing circuit according to claim 15, further comprising an amplifier connected to an output terminal of said peak detector means for amplifying

the FM video signal with a predetermined gain after processing in said peak detector means.

20. (Original) The video signal processing circuit according to claim 15, wherein the mode information comprises SP/SLP mode information relating to operation of the VCR.

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None.